REMARKS\ARGUMENTS

Entry of the above amendment and reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-10 and 21-25 are pending in this case. Claim 21 is amended herein.

The Examiner rejected claims 21-25 under 35 U.S.C. 112, second paragraph. Claim 21 is amended to replace "pre-metal dielectric layer" with –polysilicon/metal 1 dielectric (PMD)–. While the new term is not used in the specification, it is a term of art in the art of semiconductor processing. Evidence of this is found in Wolf, "Silicon Processing For the VLSI Era" Volume II, pages 188-189, where the term PMD is defined. Copies of the relevant pages are enclosed. As used in the art and defined in Wolf, layer 26 of Figs. 1 and 2E-2I (and as described in the specification) is clearly a PMD as now claimed. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

The Examiner rejected claims 21-25 under 35 U.S.C. 102(e) as being anticipated by Oda.

Applicant respectfully submits that amended claim 21 is unanticipated by Oda as there is no disclosure or suggestion of a PMD between the lowermost metal interconnect layer and the semiconductor substrate, the PMD comprising an at least substantially porous dielectric material doped with at least one dopant. Oda only teaches using its porous dielectric 10 above the first metal interconnect layer 7. Oda does not disclose or suggest using the porous dielectric as a PMD. In fact, Oda shows a first insulating layer 4 below a first wiring layer 7 but does not disclose or suggest that this layer is or should be a

porous dielectric doped with at least one dopant. Accordingly, Applicant respectfully submits that claim 21 and the claims dependent thereon are unanticipated by Oda.

The Examiner rejected claims 1-3, and 5 under 35 U.S.C. § 102(e) as being anticipated by Oda (U.S. 6,316,833).

Applicant respectfully submits that claim 1 is unanticipated by Oda as there is no disclosure or suggestion in Oda of a porous dielectric material doped with at least one dopant located between the semiconductor device and a contact layer operable to provide electrical connection to the semiconductor device. Oda teaches a porous dielectric layer doped with fluorine. However, the porous dielectric layer 10 is used above the first metal interconnect layer 7, not inwardly of the first metal interconnect layer 7. While the porous dielectric layer 10 of Oda is located inwardly of the second metal interconnect layer 16, interconnect layer 16 is not operable to provide electrical connection to the semiconductor device as required by the claim. Therefore, there is no disclosure or suggestion in Oda of a porous dielectric layer doped with fluorine located between a semiconductor device and a contact layer that provides electrical connection to the semiconductor device. Interconnect layer 16 and via 15 provide electrical connection to interconnect layer 7, not a semiconductor device as required. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Oda.

The Examiner rejected claims 4 and 6-10 under 35 U.S.C. § 103(a) as being unpatentable over Oda (U.S. 6,316,833) in view of Tseng (U.S. 5,728,618).

Applicant respectfully submits that claims 4 and 6-10 are patentable over Oda in view of Tseng for the same reasons discussed above relative to claim 1

from which claim 4 depends. Tseng is added to teach a FET as a semiconductor device structure.

Applicant respectfully submits that claim 6 is further patentable over the references as there is no disclosure or suggestion in the references of porous dielectric material doped with at least one dopant located between the semiconductor substrate and a contact layer operable to provide electrical connection to the source and drain regions. Oda teaches a porous dielectric layer doped with fluorine. However, the porous dielectric layer 10 is used above the first metal interconnect layer 7, not inwardly of the first metal interconnect layer 7. The dielectric layer 4 of Oda is located inwardly of the first metal interconnect layer 7. Dielectric layer 4 is not taught as being porous. While the porous dielectric layer 10 of Oda is located inwardly of the second metal interconnect layer 16, interconnect layer 16 is not operable to provide electrical connection to the source and drain regions as required by the claim. Accordingly, Applicant respectfully submits that claim 6 and the claims dependent thereon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-10 and 21-25. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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complexity and loss of topological planarity, there are several other concerns.

First, new materials must be used, which necessarily involves an extensive characterization of their properties to ensure that they are compatible with all other aspects of the process technology.

Second, new process-related manufacturing difficulties may be encountered that can adversely impact manufacturing yield (e.g., interlevel shorts due to pinholes; stringers due to incomplete etching over severe steps; failure to open vias due to difficulty in implementing reliable endpoint-detection techniques in the dry-etch process; film delamination due to poor adhesion or high stress; and difficulty in bonding to some metal alloys).

Third, new failure modes may be encountered – for example, electromigration, corrosion, and hillock formation – and these must also characterized to determine whether they will significantly compromise circuit reliability.

The problems related to multilevel interconnects is listed at this point in order to show that the benefits can be gained only by successfully pursuing a considerable technical-development effort. More specific details on these problems (and on how they can be overcome) will be provided throughout the chapter. Section 4.7 also gives an overview of the yield and reliability problems that occur when multilevel-interconnect technologies are implemented.

4.2.3 Terminology of Multilevel-Interconnect Structures

Figure 4-7 shows the terminology associated with a double-level-metal structure for MOS technologies. The MOS structure has a dielectric layer between the polysilicon gate/interconnect level and Metal 1, which we refer to as the *polysilicon/Metal 1*

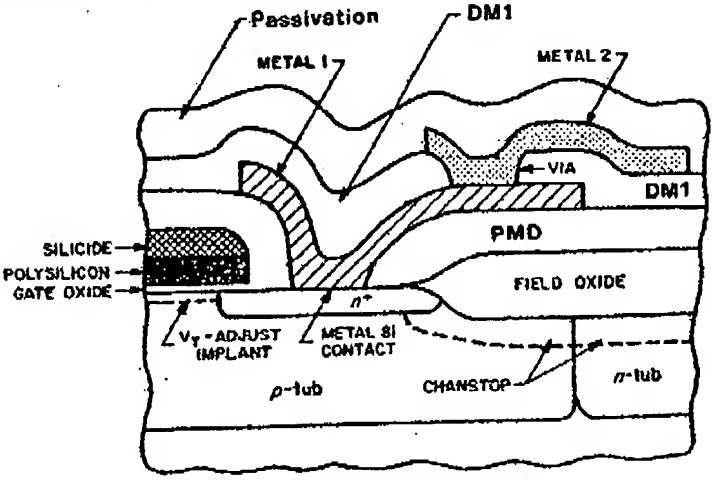

Fig. 4-7 Terminology of double-level-metal interconnects.

dielectric (or PMD). The dielectric layers between metal levels are called *intermetal dielectrics*. The intermetal dielectric between Metal 1 and Metal 2 is designated as DM1, and dielectric layers between other levels of metal (e.g., Metals 2 and 3, or Metals 3 and 4) are DM2, DM3, etc. The openings in PMD are referred to as *contact holes*. Contact through them is established between Metal 1 and polysilicon, as well as between Metal 1 and the Si substrate. Openings in the intermetal dielectric layers are known as *vias*: these allow contact to be made between Metals 1 and 2, Metals 2 and 3, etc.

In bipolar technology, the dielectric layer between Metal 1 and the substrate is still referred to as PMD, despite the fact that it may not isolate Metal 1 from polysilicon. The openings in PMD are again called contact holes, although they are only used to allow contact to be established between Metal 1 and the substrate (i.e., not poly). The notation for the other metal and dielectric layers is otherwise identical to that used in MOS technologies.

A distinction exists between our use of the terms *multi-level* and *multilayer*. A *multilayer-interconnect structure* is a thin film consisting of more than one layer of material, but existing at just one level of the interconnect system. Hence, a multilayer film can serve as the conductor (or dielectric) at each level of a multilevel-interconnect system.

4.3 MATERIALS FOR MULTILEVEL INTERCONNECT TECHNOLOGIES

The two groups of materials employed in multilevel-interconnect technologies are *thin-film conductors* and *thin-film insulators*. In this section we will describe the properties of such materials that have been adopted for use in VLSI applications.

4.3.1 Conductor Materials for Multilevel Interconnects

4.3.1.1 Requirements of VLSI Conductor Materials. Before describing properties of the specific conductor materials that have been considered for VLSI interconnect technologies, it's useful to examine the general requirements needed by such conductors. The most important of these are listed in Table 4-2. The list is long and many of the requirements are quite stringent. Nevertheless, unless a conductor structure can satisfy virtually satisfy all of them, it is unlikely to find use in VLSI applications. As a result, the number of materials that have been found suitable for VLSI interconnects is rather small. Table 4-3 summarizes the important properties of this group. The resistivities given in the table are typical for polycrystalline films with thicknesses of 10 - 1000 nm. The lower-resistivity values are exhibited by films that are purer and thicker, and that are large-grained. Deviations from stoichiometry for alloy conductors usually also lead to increased resistivity. As a result, the resistivity of a given type of film may vary from one deposition run to another, unless all deposition parameters are controlled to yield identical films.

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